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A DIGITAL MICRO-TESLAMETER

K.R. Dickson and P. Galbraith

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ABSTRACT

The instrument described is designed to measure homogeneous magnetic fields in the range -0.5 T to +0.5 T with a precision of 10^{-4} and a resolution of 5 μT. This is accomplished, on a single range, by the use of solid-state components and a.c. techniques to excite the transducer (a Hall-effect probe) and recover the resulting signal. The excitation and detection modules are described in detail; the remaining modules (microprocessor controller, interface circuitry) are based on existing hardware.

A calibration procedure using a high-stability electromagnet, a special-purpose program and a zero-field chamber allows the Hall voltage to be converted directly to units of magnetic-flux density, using a stored calibration curve. Drift of d.c. offsets in the detector analog and analog-to-digital conversion stages may be corrected for by an internal calibration routine.

The instrument may be controlled locally by means of front panel switches or remotely by a general-purpose interface bus controller.

CONTENTS

1. INTRODUCTION

The micro-teslameter has been developed principally for use in the LEP field-display system. In many respects, it is a development of the earlier d.c. system designed by Brand and Brun [1], but an a.c. excitation and detection system has been adopted to allow a measurement precision of 10^{-4} of full scale (0.5 T) or 5 μT (whichever is larger) to be obtained. Laboratory measurements of magnetic fields have been made with alternating current techniques for some time [2,3]; modern semiconductor technology allows the technique to be used as the basic operating principle of a field-measuring instrument.

The increased sensitivity of the system has meant that the component temperature drift and the device noise have had to be maintained within strict limits. An automatic calibration system has been included to allow for the long-term variation of hybrid components.

The instrument may be controlled locally or remotely by a minicomputer and digital bus and, after a warm-up period for the probe and electronics, can perform one measurement per second, or five per second on a less sensitive range.

2. PRINCIPLE OF OPERATION

A Hall plate is used as the sensitive element and is mounted on a temperature-controlled copper block similar to that described in Ref. 1. The block is maintained at a constant temperature within a few hundredths of a degree centigrade for an ambient variation from 15 °C to 30 °C.

The measuring head with Hall plate is connected by a dual cable of 10 m length to the instrumentation crate containing the electronic circuitry. This consists of a temperature-control unit, an a.c. constant-current source, a synchronous detector, a voltage-to-frequency converter with counter circuitry, and of a microprocessor, a memory, and interface boards (Fig. 1).

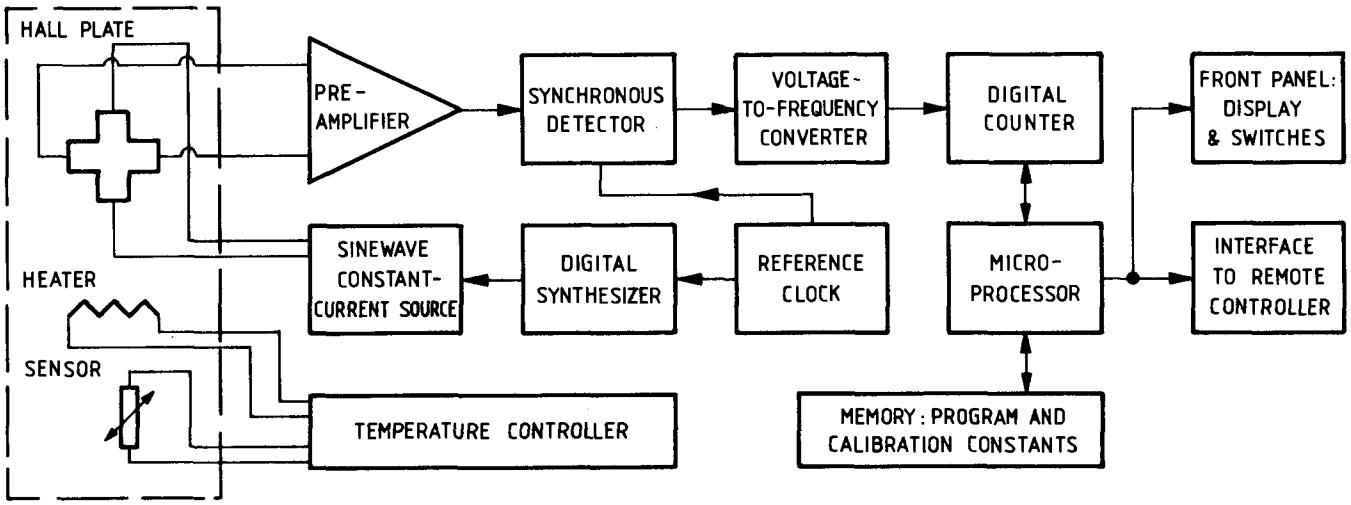


Fig. 1 Block diagram of the digital micro-teslameter

The digitized Hall voltage is converted to a field value using a set of calibration coefficients which are stored in a read-only memory (EPROM). The measurement may thus be displayed directly in physical units, e.g. in gauss or tesla.

The instrument is equipped with the IEEE-488 general purpose interface bus (GPIB) and may, therefore, be controlled along with a group of instruments by a bus controller. All operations, e.g. triggering of a measurement and read-out of the result, may be performed remotely.

3. PRINCIPLES OF DESIGN OF THE HALL-VOLTAGE DETECTOR

3.1 Overview

The measurement of magnetic fields below 100 μT with a Hall-effect transducer involves the accurate measurement of signals of less than 1 μV (Section 3.3.1). This is at the lower limit of detection for d.c. systems and, therefore, a.c. systems must be considered.

When measuring a 5 μT field in a bandwidth of 700 Hz, the signal-to-noise ratio on the transducer output is of the order of 36 dB (Sections 3.3.1 and 3.3.2). The transducer source impedance (20 Ω) poses matching problems, and the customary solution of transformer matching was rejected on account of the linearity sought. Direct connection to a low-noise operational amplifier will cause a reduction in the signal-to-noise ratio of typically 30 dB to give a signal 6 dB above noise on the filter output.

A filter system comprising a band-pass input and a narrow-band output filter was considered. An input stage with resistor/capacitor coupling to the Hall plate will exhibit a signal-to-noise ratio on the first stage output of typically -33 dB (Section 3.4.) due to the noise mismatch between amplifier and source. A narrow-band second stage permits recovery of the signal; a signal-to-noise improvement factor of 41 dB will give a signal 8 dB above noise on the detector output. This system depends, though, on the stability of the filter bandwidth. The criteria for the output filter (6 Hz passband about a signal frequency of 400 Hz) led to this scheme being rejected in favour of a system based on synchronous detection.

Demodulation to d.c. with a synchronous demodulator, which has an effective output-stage bandwidth of 1 Hz, and an integrator, is considered to be a superior method. The improvement factor of such a system (53 dB) is enough to provide a signal-to-noise ratio on the detector output of 20 dB for a minimum field of 5 μT.

Measurements have shown that a resolution of 1 μT is possible; component drift limits this to a working specification of between 5 and 10 μT.

3.2 Hall-effect transducer

The Siemens SBV 585-S1 Hall plate is used. By comparison with the plate (SBV 579) used in the teslameter of Brand and Brun it has a lower temperature coefficient of Hall voltage, thus permitting an increase in measurement resolution. The active area is smaller and the sensitivity is approximately half that of the SBV 579. The principal specifications are shown in Table 1.

TABLE 1

Principal specifications of Hall plate SBV 585-S1

Material	Indium arsenide (InAs)
Maximum driving current	100 mA
Sensitivity	$\geqslant 0.5\ V \cdot A^{-1} \cdot T^{-1}$
Temperature coefficient of Hall tension	$0.7 \cdot 10^{-4}$ per °C

3.3 Design of detector input stage

Using the specified driving current and detector input stage, the signal corresponding to a field of 5 μT is buried in noise to -33 dB.

3.3.1 Minimum Hall signal

The Hall plate generates a potential V_h in the presence of a magnetic field B, according to

$$V_h = K_{BO} \cdot I_1 \cdot B .$$

For the Siemens Hall plate SBV 585-S1, $K_{BO} = 0.5\ V \cdot A^{-1} \cdot T^{-1}$. For a minimum field of B = 5 μT, and with an excitation current of I_1 = 50 mA r.m.s., the minimum Hall signal is 125 nV r.m.s.

3.3.2 Equivalent noise resistance of a Hall plate

Burkhardt and Strutt [4] measured the equivalent noise resistance of a sample of InAs, using a d.c. excitation current of 100 mA, in the presence of a magnetic field. With fields of 0.6 T and 100 μT, they measured, at a frequency of 500 Hz, noise equivalent resistances of 30 Ω and 10 Ω, respectively. The noise is due to

- thermal noise, which has a constant spectral density,
- 1/f noise, which has a noise-power spectrum inversely proportional to frequency f and originates from charge carriers whose average lifetime is not constant, and
- a noise component defined as Hall noise, which originates from the altered spatial distribution of fluctuations of charge-carrier density in the presence of a magnetic field.

For the purpose of signal-to-noise ratio calculations, an equivalent noise resistance of

$$R_{EQ} = 20\ \Omega$$

will be used later for the plate SBV 585-S1.

3.3.3 The detector input

Details of the detector input are shown in Fig. 2. A signal frequency of 393 Hz was adopted. This frequency is high enough for the signal to be out of the range of 1/f noise, the upper limit being set by the rate at which the digital synthesizer may be driven (Section 4.2).

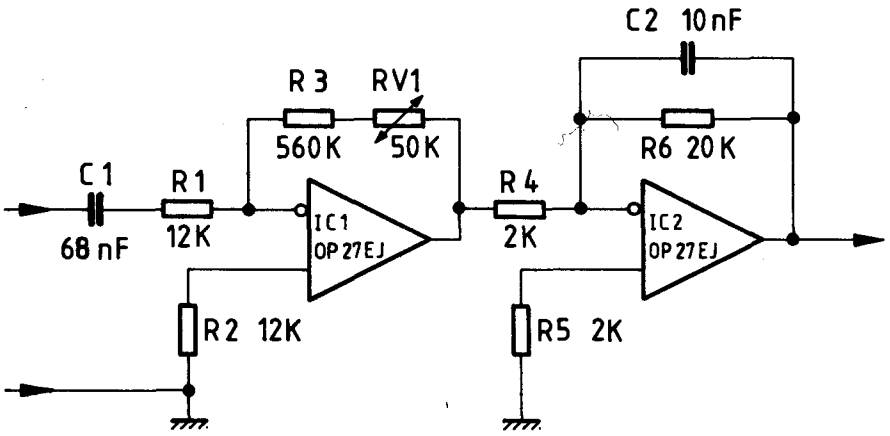


Fig. 2 Input stage of the detector

The two input stages of the detector give a band-pass characteristic with upper and lower 3 dB points at frequencies f_1 = 200 Hz and f_2 = 800 Hz, thereby forming a passband around the signal frequency. The gains of the first and second stages are 30 and 7, respectively.

For optimum noise matching, and thus minimal loss of signal-to-noise ratio, a low-impedance input network ($\sim$ 1.5 kΩ) is required. The input stage resistance and capacitance product is determined by the time constant of the high-pass response. A capacitor with a temperature coefficient of the order of 10^{-4}/°C or better was required. A metallized polysulphone device was selected; space restraints set an upper limit to the physical size of the device, thus determining its capacitance and hence the value of the resistor.

3.3.4 Signal-to-noise ratio for minimum field signal

For an applied field of 5 μT, the Hall signal has been shown to be 125 nV r.m.s. To calculate the signal-to-noise ratio, the mean square values of signal and noise are taken; thus

$$\bar{s}^2 = A_0^2/2 ,$$

where the peak-to-peak signal is $2A_0$ (note that $s_{r.m.s.} = A_0/\sqrt{2}$).

The mean square signal is

$$\bar{s}^2 = (125\ \text{nV})^2 = 1.6 \cdot 10^{-14}\ \text{V}^2 .$$

The noise signal is taken to be the noise in a 700 Hz bandwidth (the noise bandwidth of the input filter, Section 3.4.1) due to a source resistance corresponding to the impedance of the input capacitor at the signal frequency, R_{C1}, the resistor, R_1, and the equivalent noise resistance of the Hall plate, R_{EQ} (see Fig. 3). Assuming no correlation of the noise sources, a total mean square noise of

$$\begin{aligned} \bar{n}^2 &= 4 \cdot kT \cdot \Delta f(R_{EQ} + R_{C1} + R_1), \\ &= 4 \cdot (1.4 \cdot 10^{-23})(315)(700)(18 \cdot 10^3)\ \text{V}^2, \\ &= 2.2 \cdot 10^{-13}\ \text{V}^2 \end{aligned}$$

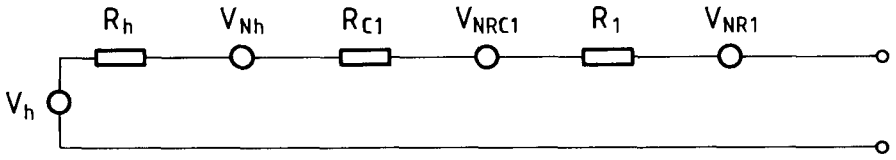
is predicted. This gives a signal-to-noise ratio at the amplifier of -23 dB.

There will be a further degradation in signal-to-noise ratio through the first amplifier stage due to the amplification of the amplifier's intrinsic voltage and current noise. The noise figure of the amplifier (F_1) quantifies this by expressing

$$F_1 = \frac{\text{(best possible signal-to-noise ratio)}}{\text{(actual output signal-to-noise ratio)}} .$$

The noise figure is, therefore, a measure of the difference between the signal-to-noise ratio attainable with a noiseless amplifier and that actually attainable when the amplifier noise is taken into account. Similarly, the second stage, with noise figure F_2, will degrade the signal-to-noise ratio further. The noise figure of a two-stage system is substantially equal to that of the first stage provided that A_1, the amplification of the first stage, and the ratio of the source impedances of the first and second stages, are both large [5].

Using the series noise resistance, R_{Nv} = 500 Ω/Hz, and parallel noise resistance, R_{Ni} = 4.14 kΩ/Hz, calculated from the data sheets [5], the noise figure from transducer-to-amplifier output, in a 700 Hz bandwidth with an 18 kΩ source impedance, was calculated to be 69 dB. The signal-to-noise ratio of 36 dB at source will, therefore, be reduced to -33 dB on the output of the first amplifier.



V_h = Hall-signal voltage generator, $V_h = K_{BO} \cdot I_1 \cdot B$,
R_h = ohmic resistance of the Hall plate,
V_{Nh} = Hall-noise voltage generator, $\bar{V}^2_{Nh} = 4 \cdot kT \cdot \Delta f \cdot R_{EQ}$, with R_{EQ} being the equivalent resistance of the Hall plate (note that $R_{EQ} \neq R_h$),
R_{C1} = real part of the capacitor impedance at the signal frequency, f_s: $R_{C1} = 1/(2\pi \cdot f_s \cdot C)$,
V_{NRC1} = noise voltage generator due to R_{C1}: $\bar{V}^2_{NRC1} = 4 \cdot kT \cdot \Delta f \cdot R_{C1}$,
R_1 = resistance of resistor R_1,
V_{NR1} = noise voltage generator due to R_1: $\bar{V}^2_{NR1} = 4 \cdot kT \cdot \Delta f \cdot R_1$.

Fig. 3 Thevenin equivalent circuit of source consisting of a Hall plate, a series capacitor, and a resistor

Assuming no correlation between the noise sources, the mean square total system noise is

$$\begin{aligned} \bar{n}^2 &= \bar{V}^2_{Nh} + \bar{V}^2_{NRC1} + \bar{V}^2_{NR1} \\ &= 4 \cdot kT \cdot \Delta f \cdot (R_{EQ} + R_{C1} + R_1) . \end{aligned}$$

3.3.5 Input common-mode rejection ratio

The operational amplifier used on the input stage has a common-mode rejection ratio (CMRR) of 125 dB, but the overall common-mode rejection of the system (i.e. amplifier and resistor network) is lower than this. Owing to the use of resistors of a maximum tolerance of 0.02 % and a closed loop gain of 30, the CMRR due to resistor mismatch is 90 dB.

The signal from the Hall probe has a common-mode amplitude of 100 mV r.m.s., and if this were to be input to a differential amplifier working with respect to a fixed ground, the system would require a common-mode rejection of 120 dB to detect a differential Hall signal of 100 nV r.m.s. This problem was overcome by powering the detector from a separate supply with a floating ground.

3.4 Signal-to-noise ratio improvement using filter techniques

Alternating-current filter techniques could, in theory, permit recovery of the signal. These are considered impractical on the grounds of stability requirements.

3.4.1 a.c. pre- and post-filter system

A detector consisting of a pre-filter of bandwidth 600 Hz and a post-filter of bandwidth 25 Hz, both centred on the signal frequency, is considered.

A measure of the effectiveness of the detector in retrieving a signal buried in noise is the improvement in signal-to-noise ratio between the input and the output of the detector. This ratio [6] is approximately equal to the reciprocal ratio of input filter noise bandwidth (B_I) to output filter noise bandwidth (B_O), i.e.

$$I = \frac{SNR_O}{SNR_I} = \frac{B_I}{B_O} ,$$

where the noise bandwidth of a filter, being greater than its 3 dB bandwidth, is that of a rectangular filter which would transmit the same amount of noise power as the original one with its particular, non-rectangular transfer function. The square-wave reference waveform generates a series of harmonic transmission windows centred on odd harmonics of the reference frequency, but it is assumed that these do not contribute to the output noise since the input noise is band-limited.

The noise bandwidth may be written as

$$f = \frac{1}{A_{V0}^2} \int_0^\infty [A_V^2(f)] \, df ,$$

where $A_V(f)$ is the network voltage gain as a function of frequency and A_V is the peak network voltage gain [7].

The noise bandwidth of the input stage of the detector was estimated graphically, from a plot of voltage gain squared against frequency, to be 700 Hz.

An output band-pass filter of bandwidth 25 Hz, centred on a signal frequency of 400 Hz, has a noise bandwidth [8] of

$$B_O = \frac{2\pi f}{4Q} ,$$

giving, for Q = 100,

$$B_0 = 6 \text{ Hz} .$$

These figures may be used to calculate the estimated improvement factor of the detector:

$$I = \frac{700 \text{ Hz}}{6 \text{ Hz}} = 117 = 41 \text{ dB} .$$

This detection system would thus be capable of recovering the Hall signal corresponding to a field of 5 μT buried in noise to -33 dB (Section 3.3.4) to give a signal-to-noise ratio of approximately 8 dB at the detector output.

In practice, a higher signal-to-noise ratio on the output is required. In addition, the stability requirements of a high-Q filter at this frequency are difficult to meet. For these reasons, the possibility of using a more refined system, based on synchronous detection, was explored.

3.5 System based on synchronous detection

After band-pass/amplification, the signal is demodulated to d.c. with a phase-sensitive rectifier. A low-pass filter and a digital integration stage allow the output of a count proportional to the peak a.c. signal level. This system makes it possible to obtain a resolution of 1 μT.

3.5.1 The amplitude detector

The basis of the amplitude-measuring system is a synchronous reversing switch which operates on the principle utilized in phase detectors based on a ring demodulator or synchronous detector. The switch is a two-state system and is controlled by a pulse train derived from the reference signal, but the phase is shifted slightly to allow for any phase shift of the sine-wave signal through the cable network.

The amplitude-measuring function of the detector and the demodulation methods used in double side-band (DSB) detection of amplitude-modulation communication systems are similar in function. In our case, the problem of synchronizing the pilot carrier, i.e. the signal to the synchronous switch, does not arise. The basic theory of DSB detection is nevertheless applicable and it is useful to note that the process of synchronous detection yields a 3 dB gain from pre- to post-detector due to the fact that a proportion of noise signal is in phase quadrature with the desired signal and is thus removed during the process of synchronous detection [9].

The Hall signal is applied to a follower and an inverting amplifier. Low-noise, low-drift devices were chosen for this purpose. At this stage, the field signal ranges from 55 μV to 5.5 V r.m.s. corresponding to a field range of 5 μT to 0.5 T. A solid-state switch selects an output from these amplifiers alternately to provide a full-wave rectification of the signal output. The analog switch is a complementary metal-oxide (CMOS) device and exhibits characteristics, such as low 'ON' resistance, low leakage, and fast switching times, which approach those of the ideal switch. The device is fabricated using a combination of bipolar and CMOS technology, allowing the utilization of a transistor-transistor logic (TTL) compatible drive stage.

This system allows a high dynamic range of signal amplitudes to be handled, the range of Hall voltage which corresponds to fields from 5 μT to 0.5 T being equivalent to a range of 100 dB.

The magnitude of the full-wave rectified signal on the switch output was estimated by representing the reference waveform by the Fourier series

$$r(t) = \frac{4}{\pi}\left[\sum_{n=1,3,5}^{\infty} \frac{(-1)^{(n+3)/2}}{n} \cdot \cos n\left(\omega_R t + \phi_R\right)\right],$$

and the input signal by

$$s(t) = \sqrt{2}\, V_S \cos\left(\omega_S t + \phi_S\right) ,$$

where V_S is the r.m.s. value of s(t) and $\sqrt{2}\, V_S$ the peak amplitude.

The switch operation is to multiply effectively s(t) by r(t) to give the product

$$V_p(t) = r(t) \cdot s(t) .$$

The output of a low-pass filter on the switch output may be estimated by multiplying term by term, setting $\omega_S = \omega_R$ for synchronous operation, assuming that the two signals have zero phase difference and that the filter cuts off at well below the reference frequency. The filter output will be of the order of:

$$V = \frac{2\sqrt{2}}{\pi}\left[V_S \cdot A_L(0)\right] ,$$

where V_S is the r.m.s. signal amplitude and $A_L(0)$ the magnitude of the filter response at zero frequency.

The a.c. signal on the detector input has thus been converted into a d.c. voltage which is proportional to the amplitude of the signal.

It should be noted that the detector is harmonically responding, i.e. the detector will give a d.c. output in response to signals at frequencies $3\omega_R$, $5\omega_R$, etc., but the relative sensitivity of detection at these frequencies corresponds to the relative magnitudes of the reference Fourier components (1/3, 1/5, etc.). Filtering of the constant-current signal and on the input stages of the detector may alleviate this problem. The adoption of a sine-wave signal reference is the only possible method of avoiding it.

An integration period of 1 s was used. The noise bandwidth of a low-pass filter with a 1 Hz cut-off frequency is 1.6 Hz. The improvement factor for the synchronous detector is thereby estimated to be

$$I = \frac{700\ \text{Hz}}{1.6\ \text{Hz}} = 438 = 53\ \text{db} .$$

It was estimated that the detector would be capable of recovering the signal buried in 33 dB of noise to give a signal-to-noise ratio of 20 dB on the output. In practice, a resolution of 1 μT was observed.

3.5.2 Detector full-scale sensitivity

The detector is designed to give a d.c. output V_O in response to an in-phase sine wave with an r.m.s. value of V_S. The general relationship between V_O and V_S is

$$V_O = V_F \left(\frac{V_S}{S_F}\right) \cos \phi ,$$

where V_F is the full-scale output voltage, S_F is the full-scale signal channel sensitivity, and ϕ is the phase difference between the Hall signal and the reference signal.

The full-scale sensitivity S_F measured from the signal channel input is the r.m.s. value of an in-phase synchronous sine wave which gives a full-scale d.c. output. The design value of S_F corresponds to the maximum field measurable, 0.5 T, and is, from Section 3.2:

$$S_F = V_{h,max} = (0.5)(0.05)(0.5) = 12.5 \text{ mV r.m.s.}$$

The detector full-scale sensitivity S_D is defined from

$$S_D = S_F \cdot G_A ,$$

where S_F is defined above and G_A, the signal channel gain, is set to approximately 210. The detector sensitivity S_D is thus 8 V r.m.s.; V_F, set by the maximum input to the voltage-to-frequency converter (VFC), is 5 V, and ϕ, the phase difference between signal and reference, is set to zero using dual-in-line switches on the reference electronics.

The equation for the output voltage V_O of the detector is, therefore, with no phase difference:

$$V_O = 5 \cdot \frac{V_S}{0.0125} = 400\ V_S ,$$

where V_O is in volts d.c. and V_S is in volts r.m.s.

3.5.3 Digital output stage

The output of the low-pass filter ranges from -5 V d.c. to +5 V d.c., corresponding to fields from -0.5 T to +0.5 T. A two-stage conversion process is used to allow the digital display of the magnitude of the field. A VFC converter is used to convert the voltage into a train of constant width and constant amplitude pulses, the pulse rate of which is proportional to the amplitude of the analog signal. The pulses are counted and stored in a register which is read by the control logic.

The use of a VFC and counter to provide analog-to-digital conversion enables the integration period to be set to an integral number of signal excitation cycles, thus rejecting the noise at the signal frequency and, in theory, enabling indefinitely long integration times to be obtained. Assuming the noise on the filter output to be Gaussian, there is an inverse relationship between the averaging time and the resolution of the measurement [10].

The VFC employed is a 1 MHz unit with the input offset to mid-scale. Integration times of 0.2 s and 1 s are used, the former providing a less accurate measurement. On the 1 s range, one million counts correspond to a measured field of +0.5 T; one count, therefore, corresponds to 1 μT. The VFC gain and offset drift with temperature and with time.

A thermostatically controlled enclosure was used to limit the drift with temperature to within an indicated ± 2 μT over short time periods. A calibration system corrects for the drift of the VFC gain with time (equivalent to 5 μT per day).

3.5.4 Minimum detectable signal

Since the objective of the detector is to produce an output d.c. voltage proportional to the applied magnetic field, the d.c. performance of the system was considered. Amplifier input offset voltage, input bias currents, input offset currents, and their respective thermal drifts are the main sources of d.c. errors. Alternating current coupling is used between the Hall signal and the detector and between the input amplifier and the amplitude detector; thus only the output stages need to be considered.

The output low-pass filter has a unity gain at d.c. The limits on the stability of the filter output provide an estimate of the limits of measurement of the system.

Using figures of 0.3 μV/°C for the temperature coefficient of the offset voltage and 8 pA/°C for the offset current through a source resistance of 24 kΩ, it was estimated that the drift of the filter output voltage would be 0.5 μV/°C. Over an operating temperature range from 15 °C to 35 °C, this corresponds to a drift of 10 μV, or an indicated 1 μT. Worst case data of 1.3 μV/°C and 35 pA/°C give an output voltage drift of 2 μV/°C, or 4 μT over the operating range.

In practice, although a resolution of 1 μT is possible, the long-term drift limits the resolution of the instrument to between 5 μT and 10 μT.

4. CONSTANT-CURRENT SOURCE

An a.c. constant-current source is used to provide a sine-wave current drive to the Hall probe. The basic requirements for this stage are that the current has a stable r.m.s. amplitude and frequency. A counter produces a sawtooth digital ramp which addresses a sine-wave encoded EPROM. The digital sine-wave ramp is used to drive a digital-to-analog converter (DAC) producing a pure voltage reference signal which is used as input to a current-drive circuit.

4.1 Digital counter

A quartz oscillator, tuned to a frequency of 1.6097 MHz, provides the input to a 12-bit binary counter. The eight most significant bits are used to address the EPROM with a cycle frequency of 393 Hz. The counter also provides the reference waveform to the amplitude detector. Provision is made, using a comparator network, for phase shifting the reference signal with respect to the constant-current waveform. This allows any phase difference between the two (created, for example, by differing lag times through the cable networks) to be tuned to within 0.09° (1.6 mrad). Since the amplitude detector responds to the cosine of the phase difference between signal and reference, this stage introduces a negligible error to the system, the amplitude error which corresponds to 1.6 mrad being less than $2 \cdot 10^{-6}$.

4.2 Sine-wave algorithm

Sine-wave data in an EPROM memory is used to drive a 16-bit bipolar DAC which generates a stable voltage signal. The data is stored as hexadecimal numbers with the mid-range of the DAC at 7F(Hex), corresponding to 0°, a maximum at 00(Hex), corresponding to 90°, and a minimum at FF(Hex) or 270°. The data is the hexadecimal equivalent of the integral part of

$$\text{data} = \left\{\text{INT}\ \ 127 - [127 \cdot \sin\,(N \cdot 1.40625°)]\right\},$$

a complete sine-wave cycle being made in 256 steps of 1.40625° with N ranging from 1 to 256.

The resulting sine-wave has a peak-to-peak level of approximately 2.5 V with a voltage step defined to one least significant bit or 153 μV. The 16-bit DAC was chosen primarily for its low drift and low linearity error.

4.3 Output stage

The signal is passed through a buffer/filter with a low-pass frequency of 5 kHz to remove high-frequency switching transients, and drives a ground referenced constant-current source. The circuit is based on a design by B. Howland [12] and is shown in schematic form in Fig. 4.

With the reference signal set to zero ($V_{ref} = 0$) and all of the resistors set to the same value R (i.e. R1 = R2 = R3 = R4 = R), the current I_{load}, flowing into the load R_{load}, is proportional to the signal level V_{sig} (Appendix 1):

$$I_{load} = \frac{V_{sig}}{R}\ .$$

Tests were made on a current-source prototype using the relationship expounded in Eq. (A1.7). Using high-stability resistors with a value of 2 Ω and 4 Ω to simulate the Hall plate, the linearity of the relationship, temperature stability, and power supply sensitivity were tested. Using seven discrete levels of V_{sig}, it was found that the relationship between V_{sig} and V_{load} held to 10^{-4}. V_{load} was found to be stable to 10^{-4} for ambient temperatures of 25 °C ± 3 °C, and the sensitivity to power-supply variation was less than 10^{-4} for a variation of the power-supply voltage of 7 % about its operating point.

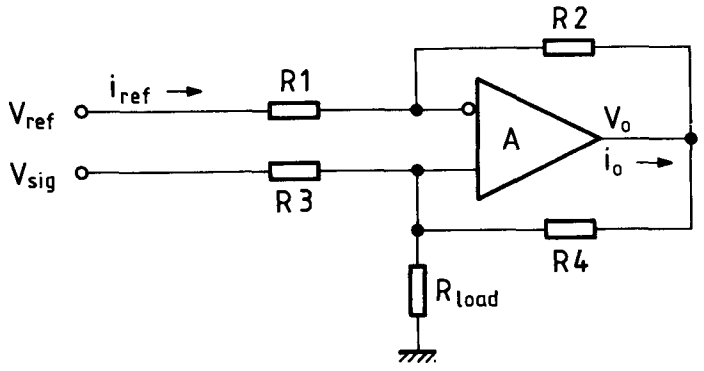


Fig. 4 Constant alternating-current source

Since the output circuit uses both positive and negative feedback, there exists the possibility that there may be some situations under which the circuit could become unstable. Some analysis was made (Appendix 2) of the circuit stability when driving a capacitive load. It was found that the system would, theoretically, be unconditionally stable. In practice, no problems with instability have been observed.

5. DIGITAL CIRCUITRY

The digital output from the VFC (Section 3.5.3) is used as input to a 24-bit counter. The counter board is interfaced to an 8-bit microprocessor bus (G-64 bus), which provides a common interface to a microprocessor card, a 24 Kbyte memory card, a display interface card and a card, which provides the interface between the G-64 bus and the GPIB. These are shown schematically, with their CERN reference numbers, in Fig. 5.

The digital circuitry is controlled by a program stored in EPROM. Also stored in memory is a set of calibration coefficients that allow the Hall voltage to be related to the magnetic induction which, for convenience, is displayed in gauss.

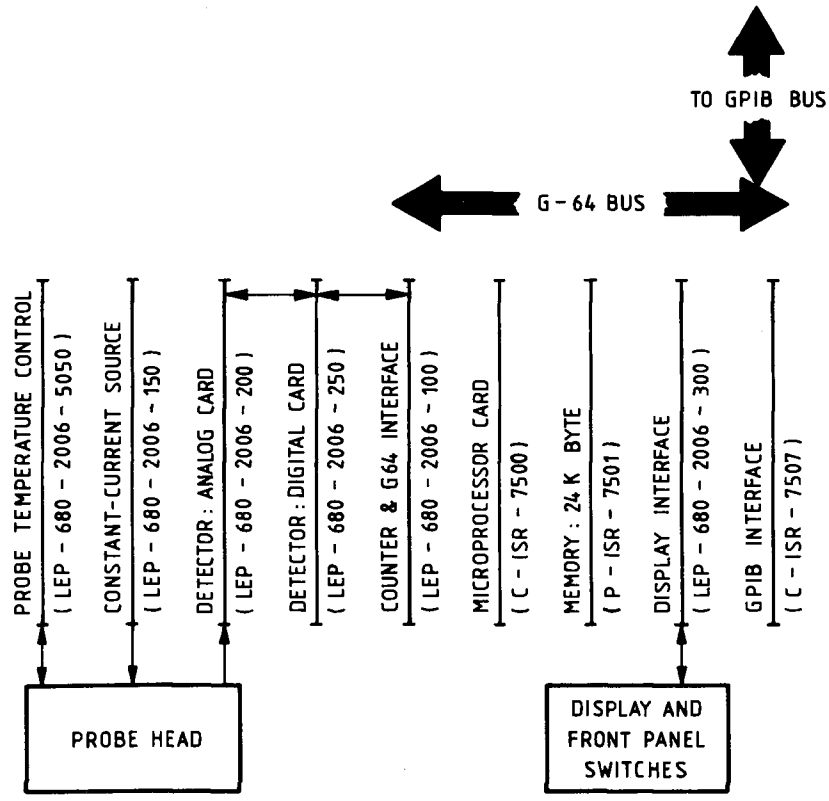


Fig. 5 Micro-teslameter in printed circuit component form

6. THE CONTROL PROGRAM

The program consists of three parts: a main program which controls the instrument, whether under local or remote control (Fig. 6), an initialization routine which sets the instrument to a preset state (Fig. 7a), and a status routine which allows the indication

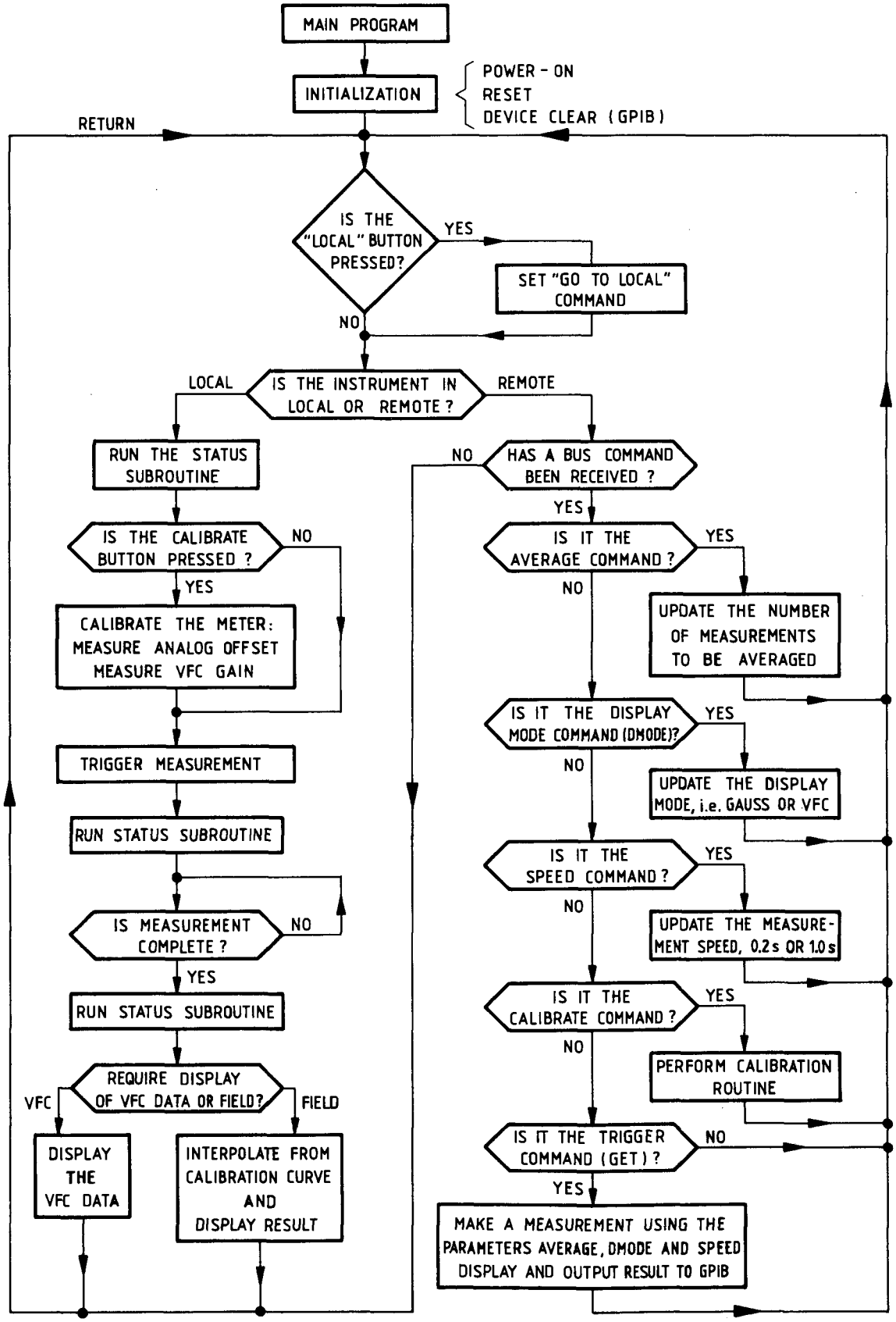


Fig. 6 Main program flow

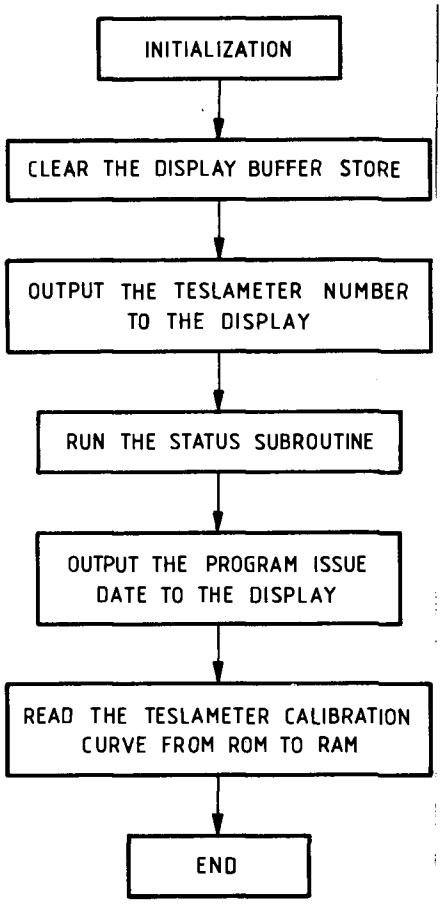


Fig. 7a Initialization routine

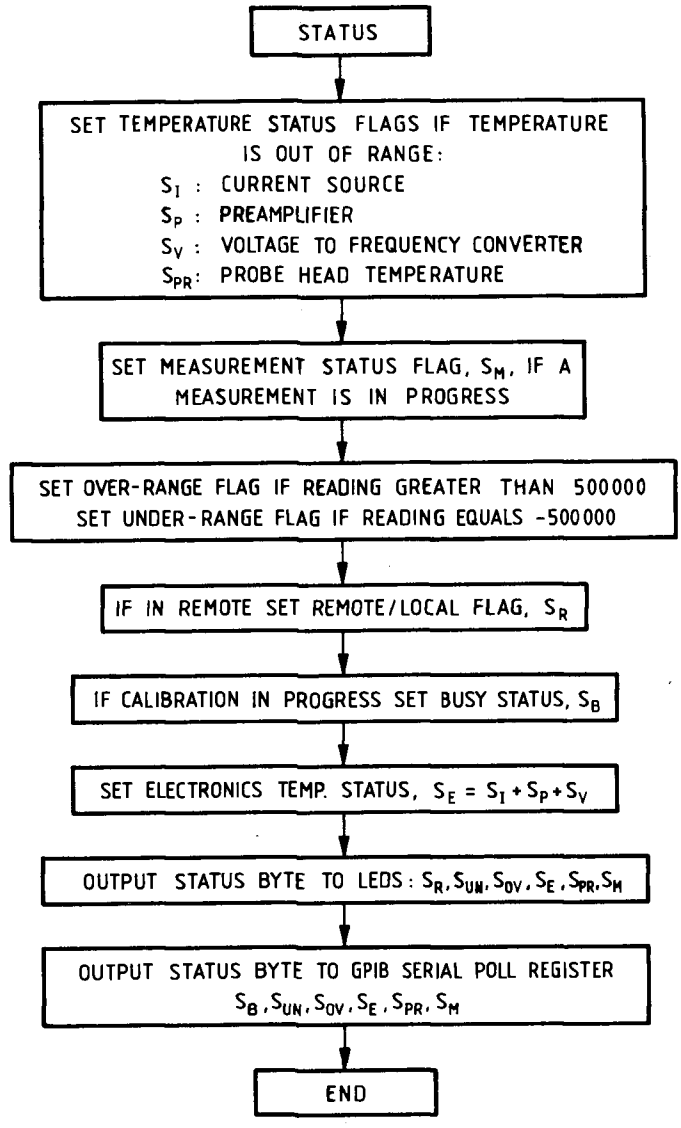


Fig. 7b Status routine

of the instrument status on the front panel light-emitting diodes (LEDS) or in a status byte over the GPIB (Fig. 7b).

The main program is built as a loop which is continuously executed, a check being made at each pass to interrogate any change of the mode of operation. In local mode, a front-panel switch allows the selection of the display of VFC reading or field value (in gauss), and push buttons enable instrument calibration or return from the remote state to be selected. In remote mode, a command buffer is interrogated for the arrival of a new command (Appendix 3). Since the instrument is designed to be controlled over the GPIB, it has a preset address assigned to it, permitting it to be used in common with other instruments by a bus controller.

7. CALIBRATION

The phase difference between the constant-current signal and the reference waveform, generated due to the presence of a low-pass filter on the synthesizer output, cable lags, etc., may be corrected by adding or removing jumpers on the current source board. The output of the switching rectifier is observed for a clean signal. A phase shift of 3° is typical. The gain of the preamplifier is set with an applied field of 0.5 T to give a full-scale indication on the display.

Ten calibration points are taken for negative fields from -0.5 T to -0.13 T and ten points for positive fields from 0.13 T to 0.5 T. A zero reference is obtained by inserting the probe into a zero field chamber (Appendix 4). A microcomputer calculates a series of calibration coefficients from a third-order spline-fitting routine. These coefficients are loaded into an EPROM memory, which is later inserted into the micro-teslameter.

During use, when the option to display the field value is selected, the field induction is derived from the Hall voltage by determining the nearest two calibration points and fitting a third-order polynomial through these points using the calibration coefficients stored in memory.

8. SPECIFICATIONS

- Hall probe current : 50 mA r.m.s.
- Range of Hall voltage : gain set by resistors, $\sim$ 30 nV to 15 mV r.m.s.
- Temperature of Hall plate : 35 °C
- Range of ambient temperature : 15 °C to 30 °C
- Full-scale reading : 0.5 T
- Precision of measurement : 10^{-4} of full scale or 5 μT
- Resolution of measurement : 5 μT
- Conversion time : 1 s, or 0.2 s giving a reading of lower precision
- Front-panel display : digital display of the result;
  status indication: remote, over/under range, electronics temperature out of range, probe temperature out of range, measurement in progress
- Front-panel switches : select display of VFC reading or gauss; calibrate; return to local
- Instrument interface : IEEE-488 (GPIB)
- Mass : 8 kg
- Power requirements : 220 V a.c., 40 W

9. CONCLUSIONS

A digital teslameter has been designed and constructed. Results have shown that an error of less than 10^{-4} of full scale (0.5 T) or 5 μT, whichever is the larger, has been obtained. The instrument can measure bipolar fields with a dynamic range of 100 dB on a single scale.

Acknowledgements

The authors would like to thank L. Resegotti and K.N. Henrichsen for the opportunity to do this work, L. Walckiers for helpful ideas and discussions, D. Lehm for supplying the Hall plates, Ch. Bugnone for constructing the zero field chamber and H. Flotow for drawing the diagrams.

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APPENDIX 1

ANALYSIS OF CONSTANT-CURRENT SOURCE

The circuit schematic for the Howland constant-current source is shown in Fig. A1.1. Using a sinusoidal test signal, the signal on the inverting terminal of amplifier (Amp. 1) will be

$$V_{inv}\, e^{j\omega t} = \frac{(V_o - V_{ref})\, R1\, e^{j\omega t}}{R1 + R2} . \qquad (A1.1)$$

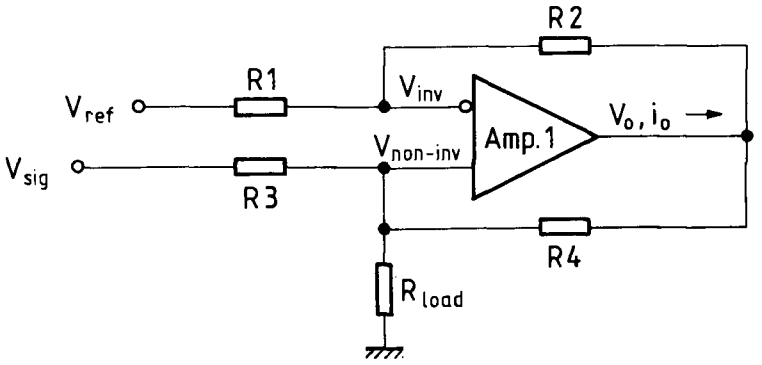


Fig. A1.1 Howland constant-current source

The general expression for a signal on the non-inverting terminal may be found from the analysis of the network in Fig. A1.2.

Since the current flowing into the amplifier input is assumed to be zero, from Kirchoff's current law:

$$(i_4 + i_{sig})\, e^{j\omega t} = i_{load}\, e^{j\omega t} , \qquad (A1.2)$$

whence

$$\frac{V_o - V_{non-inv}}{R4} + \frac{V_{sig} - V_{non-inv}}{R3} = \frac{V_{non-inv}}{R_{load}} . \qquad (A1.3)$$

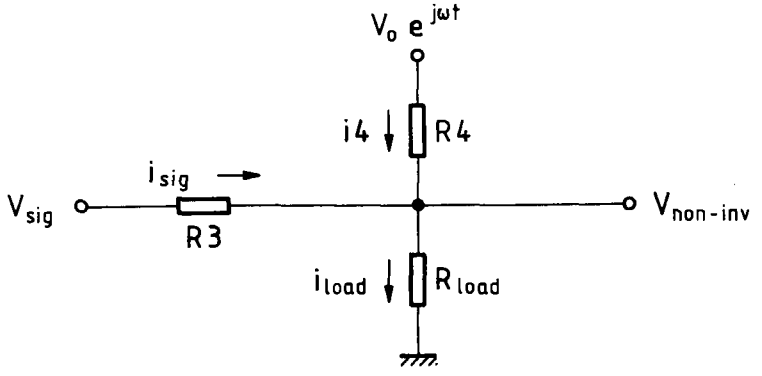


Fig. A1.2 Network on input to terminal $V_{non-inv}$

From Eq. (A1.1) it is found that

$$V_o = V_{ref} + \frac{(R1 + R2) \cdot V_{inv}}{R1} . \qquad (A1.4)$$

By rationalization of Eq. (A1.3), substituting in the expression obtained above for V_o, Eq. (A1.4), setting $V_{inv} = V_{non\text{-}inv} = V_{load}$ and R1 = R2 = R3 = R4 = R, it is found that

$$V_{load} = \frac{V_{sig} \cdot R_{load}}{R} . \qquad (A1.5)$$

Since $V_{load} = I_{load} \cdot R_{load}$, it is found that

$$I_{load} = \frac{V_{sig}}{R} . \qquad (A1.6)$$

A more general solution is obtained with

$$V_{ref} \neq 0 \quad \text{and} \quad \frac{R4}{R3} = \frac{R2}{R1} ,$$

whence Eqs. (A1.3) and (A1.4) may be solved to give

$$V_{load} = \frac{R_{load} \cdot V_{sig}}{R3} + \frac{R_{load} \cdot V_{ref}}{R4} \qquad (A1.7)$$

or

$$I_{load} = \frac{V_{sig}}{R3} + \frac{V_{ref}}{R4} . \qquad A(1.8)$$

With a constant reference voltage (V_{ref}), Eqs. (A1.6) and (A1.8) show the linear relationship between the signal V_{sig} and load current, I_{load}.

APPENDIX 2

STABILITY OF CONSTANT-CURRENT SOURCE

A circuit schematic for the constant-current source, with zero input and driving a load R_L with parallel capacitance C_L, is shown in Fig. A2.1. The characteristic equation (in the s-domain) may be found by breaking the feedback loop at point X (Fig. A2.1) and applying the signal e^{st} to the input illustrated in Fig. A2.2. The amplifier is represented by A(s), the negative feedback system by G(s), and the positive feedback system by H(s).

The amplifier response may be written as:

$$-A(s)\,[G(s) - H(s)]\,e^{st} = e^{st} \qquad (A2.1)$$

giving

$$-A(s)\,[G(s) - H(s)] = OLG(s) = 1\,. \qquad (A2.2)$$

The amplifier response may also be written as:

$$A(s) = \frac{(A_0\,a)}{(s + a)} \qquad (A2.3)$$

and, by substituting $j2\pi f$ for s, assuming an open loop gain of 10^5 and a unity gain at 50 MHz, the constant 'a' may be calculated to be 500 Hz.

The network on the inverting input of the amplifier may be analysed (Fig. A2.3) to give

$$G(s) = \frac{R1}{R1 + R2}\,. \qquad (A2.4)$$

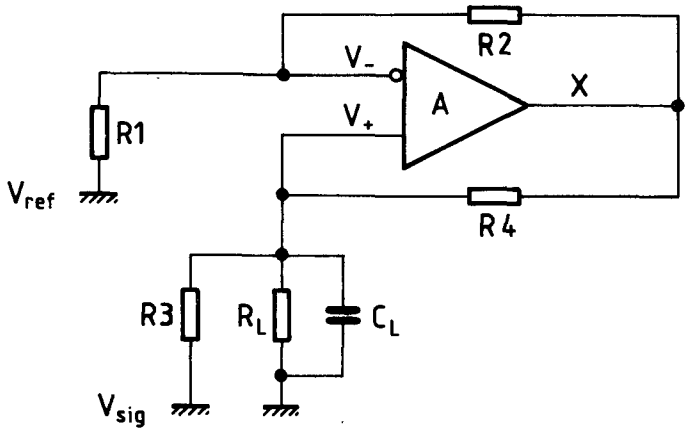


Fig. A2.1 Circuit schematic of constant-current source

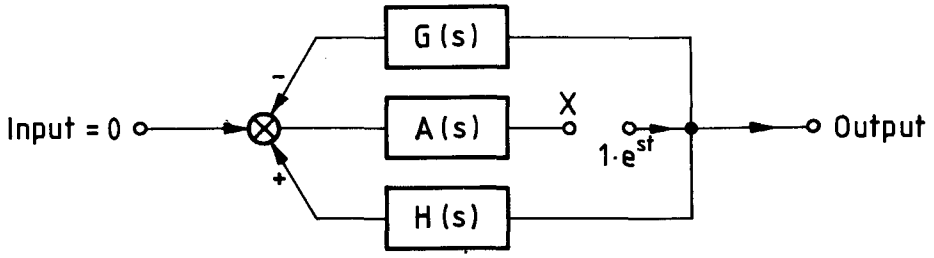


Fig. A2.2 Test for the stability of the current source

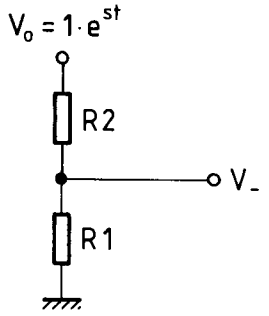


Fig. A2.3a Network on amplifier inverting input

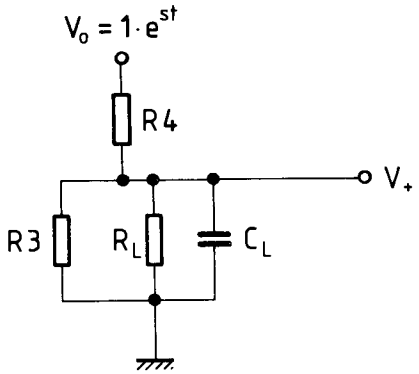


Fig. A2.3b Netwwork on amplifier non-inverting input

Similarly, H(s) may be found by analysing the network on the non-inverting input:

$$H(s) = \frac{R3 \cdot R_L}{(R3 \cdot R_L + R3 \cdot R4 + R_L \cdot R4 + sR3 \cdot R4 \cdot R_L \cdot C_L)} . \qquad (A2.5)$$

For the case where R1 = R2 = R3 = R4 = Rx, the expression for the open loop gain (OLG) reduces to

$$\frac{(A_0 \cdot a)[Rx(1 + sR_L \cdot C_L)]}{(s + a)[2(2R_L + Rx + sRx \cdot R_L \cdot C_L)]} = -1 . \qquad (A2.6)$$

Substituting the values $A_0 = 10^5$, a = 500 Hz, Rx = 23 Ω and R_L = 4 Ω reduces the expression for the open loop gain to

$$OLG(s) = \frac{-(5 \cdot 10^7)\ (23 + 92\ s \cdot C_L)}{(s + 500)\ (62 + 184\ s \cdot C_L)} = 1 . \qquad (A2.7)$$

The system is deemed unstable if any value of s satisfying

$$OLG(s) = 1 \qquad (A2.8)$$

has a positive or zero real part. The expression is mapped in the s-plane (Fig. A2.4) and it is found to be non-analytic only in the left half-plane. It is, therefore, possible to use the Nyquist graphical test for stability.

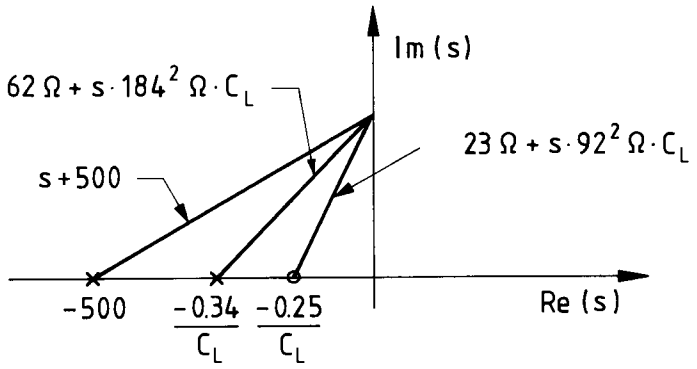


Fig. A2.4 Mapping of Eq. (A2.7) in the s-plane

Assuming that the current source has to drive a load with large capacitance (C_L = 100 µF), the modulii and arguments of the one expression in the numerator and of the two expressions in the denominator were calculated to give the modulus and arguments of the resulting expression for OLG(s), using a range of frequencies from 0 to 1 MHz. It was found that arg[OLG(s)] falls from 180° and tends to a limit at 90°. The locus of OLG(s) thus does not enter the positive portion of the Nyquist diagram. The circuit is, therefore, always stable.

APPENDIX 3

REMOTE CONTROL

GPIB commands

Command	Meaning
AVERAGE:N!	Average the reading over a number of cycles N
DMODE:GAUSS!	Set the displayed mode to gauss
DMODE:VFC!	Set the displayed mode to the VFC reading
SPEED:FAST!	Set the measurement period to 0.2 s
SPEED:SLOW!	Set the measurement period to 1.0 s
CALIBRATE!	Perform calibration
GET!	Trigger a measurement and return the result

The exclamation marks are command delimiters; carriage return and blanks are ignored by the interface.

GPIB serial poll status

S8	SRQ	S6	S5	S4	S3	S2	S1

S1 Measurement in progress
S2 Calibration in progress
S3 Probe temperature fault
S4 Electronics temperature fault
S5 Out of range
S6 Busy

S8 and SRQ (Service Request) are not used.

APPENDIX 4

ZERO FIELD CHAMBER

The zero field chamber consists of two concentric tubes of mu-metal held in a perspex support. A plastic guide channel allows the micro-teslameter probe head to be placed halfway down the tube on its central axis.

The effectiveness of the tube in shielding against transverse magnetic fields was estimated from a formula due to Mager [11], who defined a shielding factor S:

$$S = \frac{H_e}{H_i} = \frac{\mu_r \cdot d}{D},$$

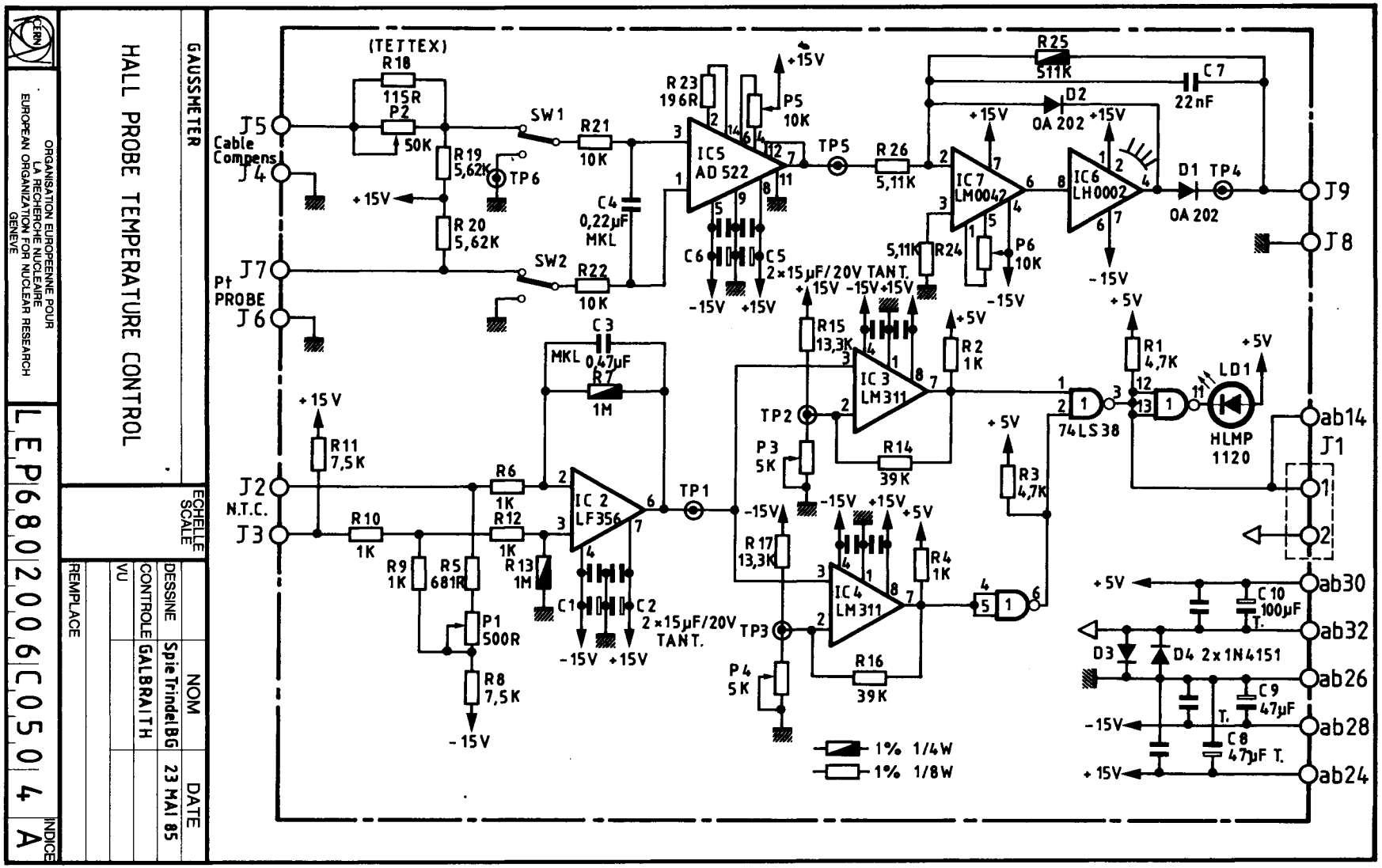
where

H_e = magnetic field strength external to the tube,
H_i = field strength inside the tube,
d = thickness,
D = diameter of the tube,
μ_r = relative permeability of the tube material.

The outer tube, of diameter 90 mm, was constructed from Permalloy B, which has a maximum relative permeability, after heat treatment, of between $1.5 \cdot 10^4$ and $4 \cdot 10^4$ at a field strength close to that of the earth's field ($40\ A \cdot m^{-1}$). The inner tube was constructed from mu-metal and has a diameter of 60 mm; this material has a maximum permeability, after heat treatment, of between $7 \cdot 10^4$ and $1.3 \cdot 10^5$.

It was observed that the remanent field inside the chamber was lower than the limit of resolution of the instrument.

SYMBOLES SCHEMATIQUES
SELON NORMES CEI
SCHEMATIC SYMBOLS
STANDARD IEC



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GENEVE

HALL PROBE TEMPERATURE CONTROL

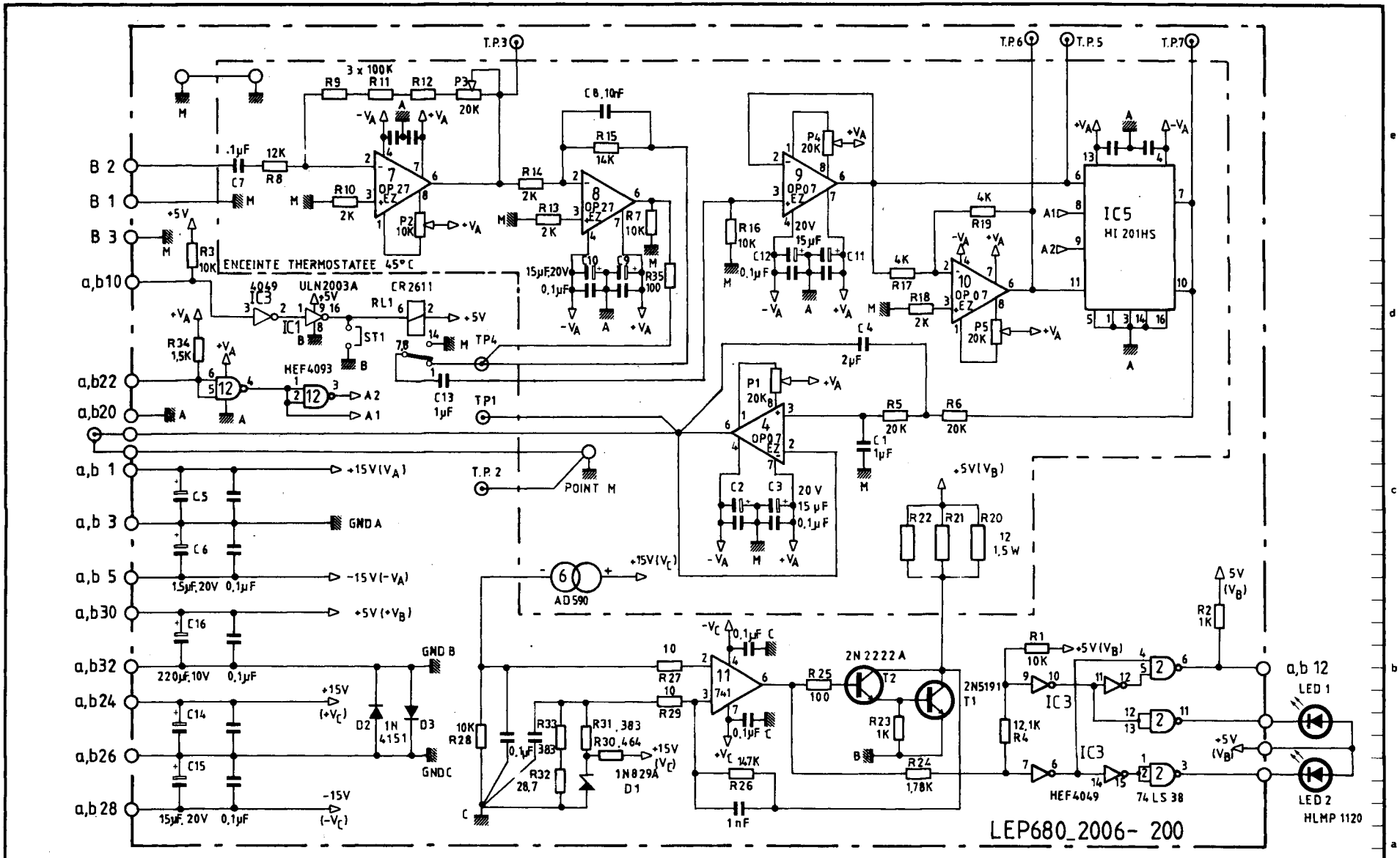
GAUSSMETER

ECHELLE
SCALE

	NOM	DATE
DESSINE	Spie Trindel BG	23 MAI 85
CONTROLE	GALBRAITH	
VU		

REMPLACE

LEP6800600C0504 A
INDICE



INDICE	DATE	NOM	ZONE	MODIFICATION

GAUSSMETER

PREAMP+SYNCHRONOUS DETECTOR

ECHELLE SCALE

	NOM	DATE
DESSINE	TRINDEL	30 octobre 84
CONTROLE	GALBRAITH	12 fevrier 85
VU		

REMPLACE

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EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH
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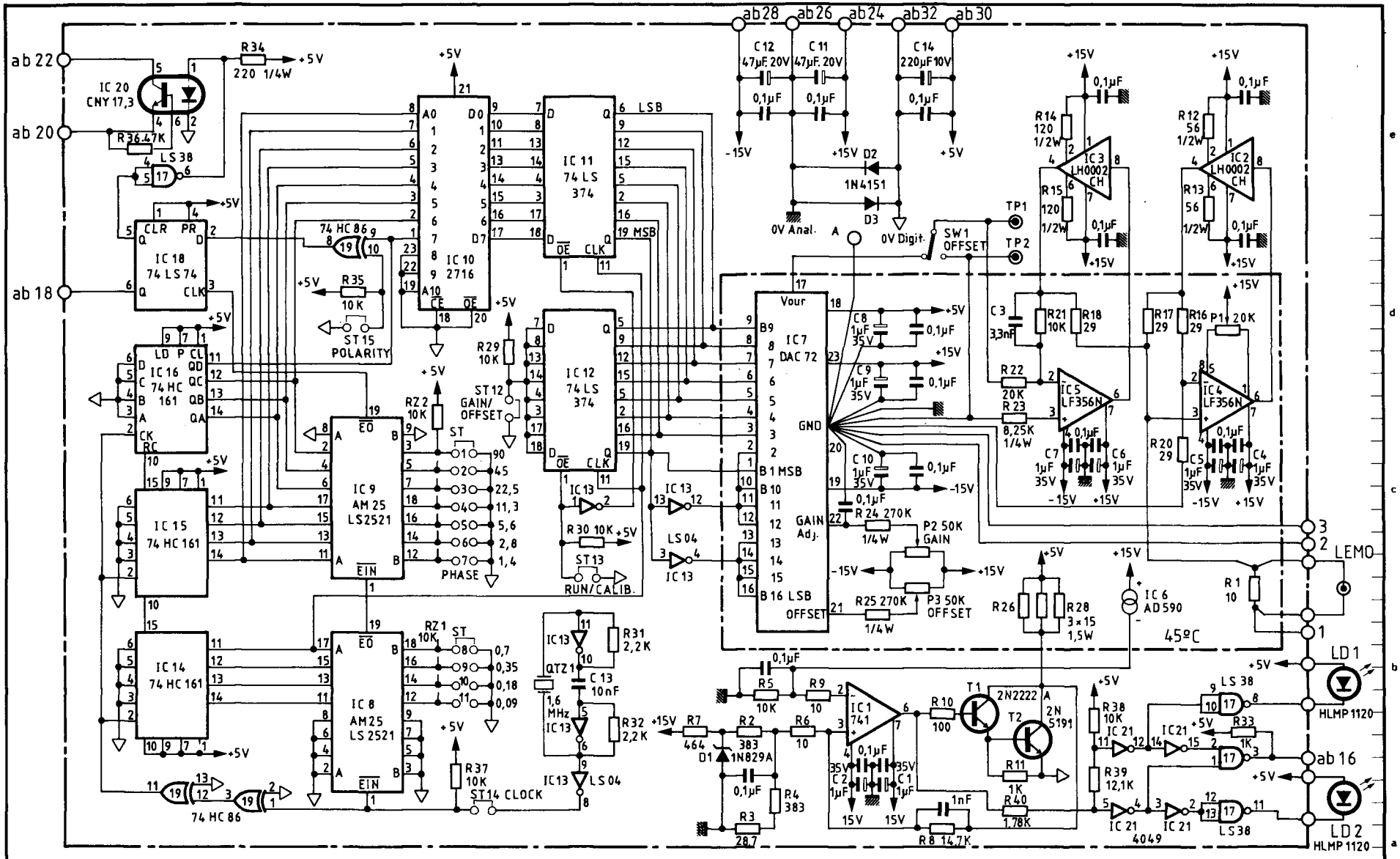
LEP680200 6C200 3 INDICE B



INDICE	DATE	NOM	ZONE	MODIFICATION

GAUSSMETER

CURRENT SOURCE

ECHELLE SCALE

	NOM	DATE
DESSINE	Spie Trindel BG	29 MAI 85
CONTROLE	GALBRAITH	12 FEV. 85
VU		
REMPLACE		

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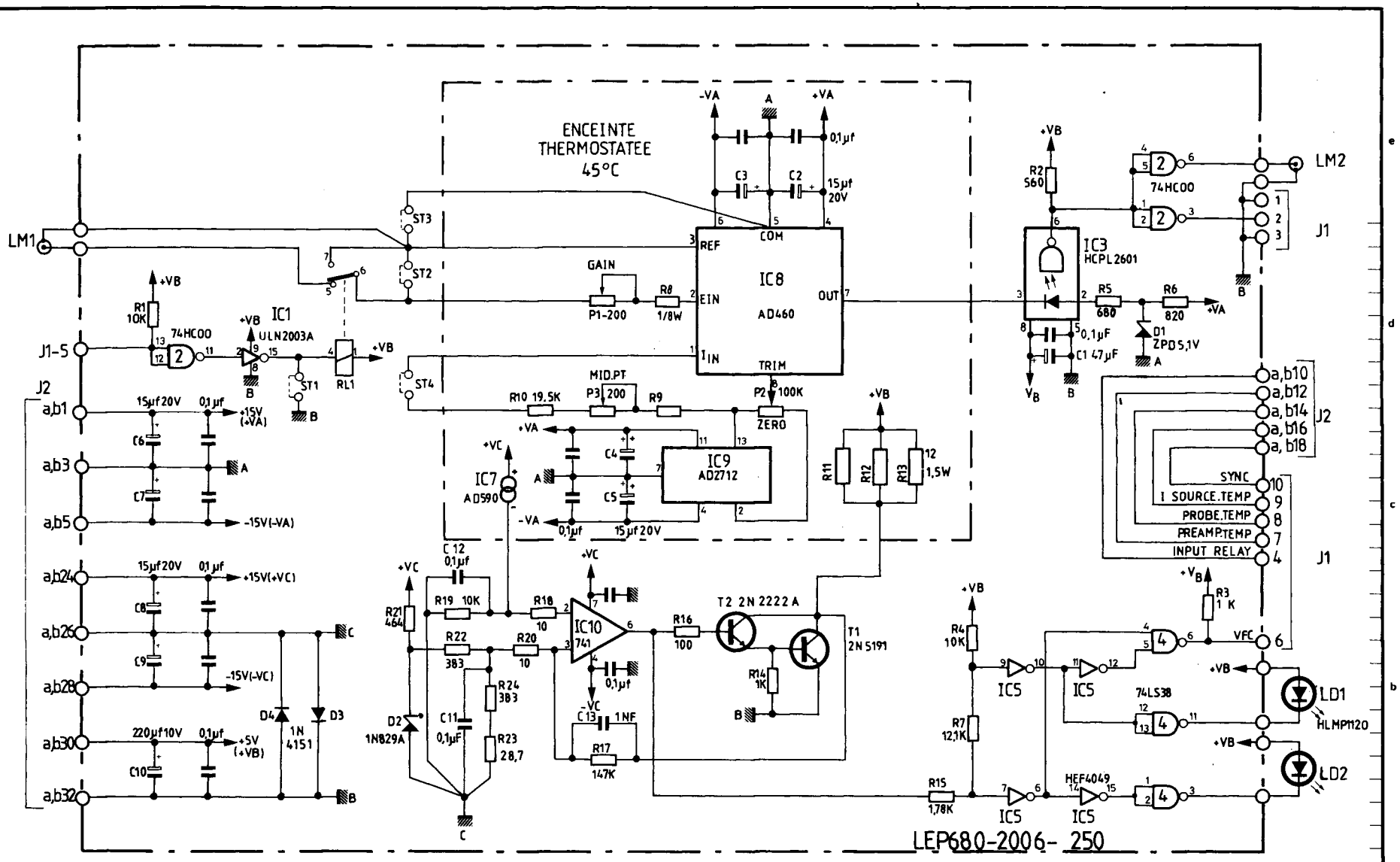
LEP 6802006 C 150 3 B

INDICE



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VtoF CONVERTOR		DESSINE	TRINDEL LG 0.5.10.84
		CONTROLE	GALBRAITH 23.11.84
		VU	
		REMPLACE	

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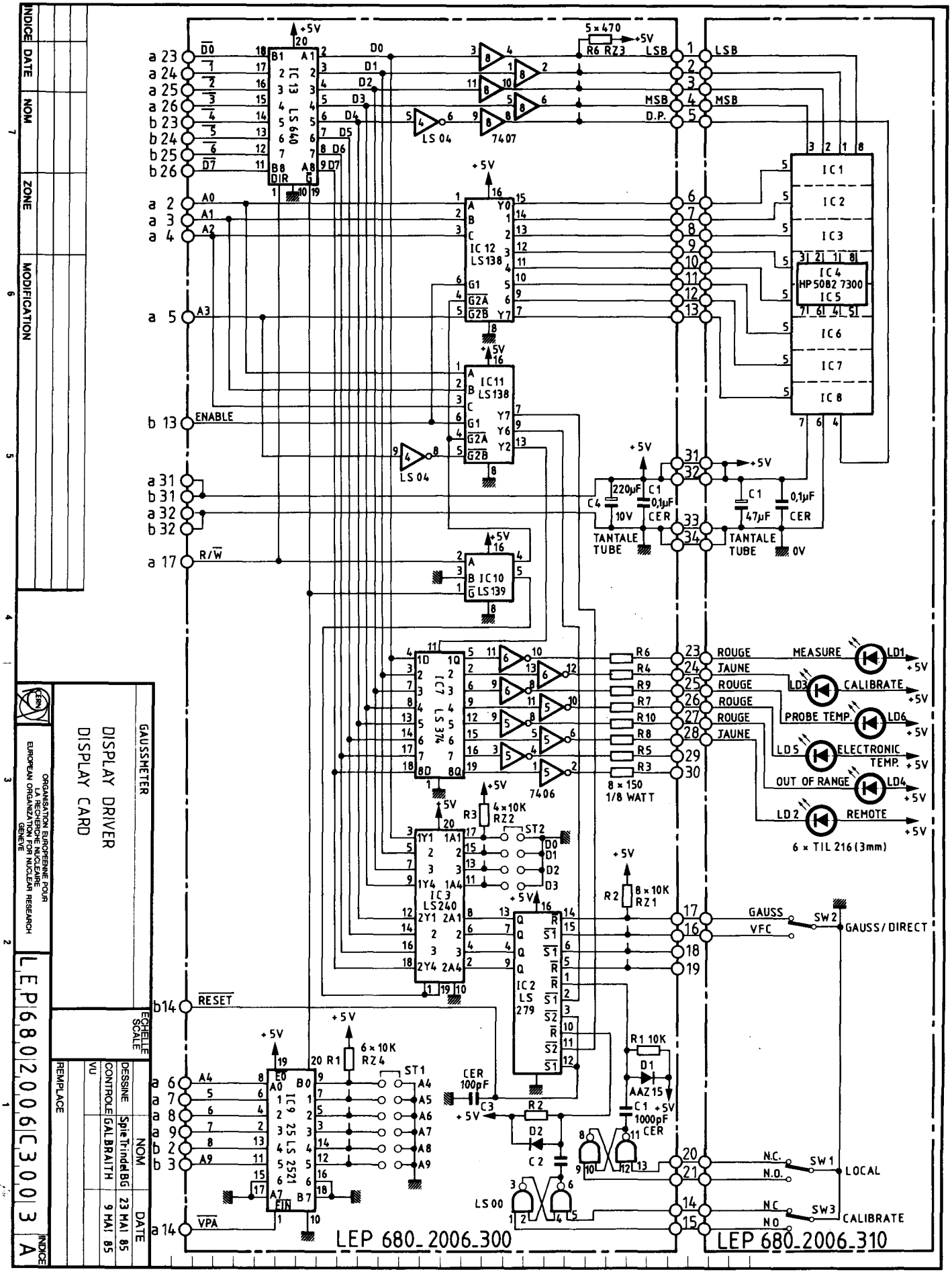
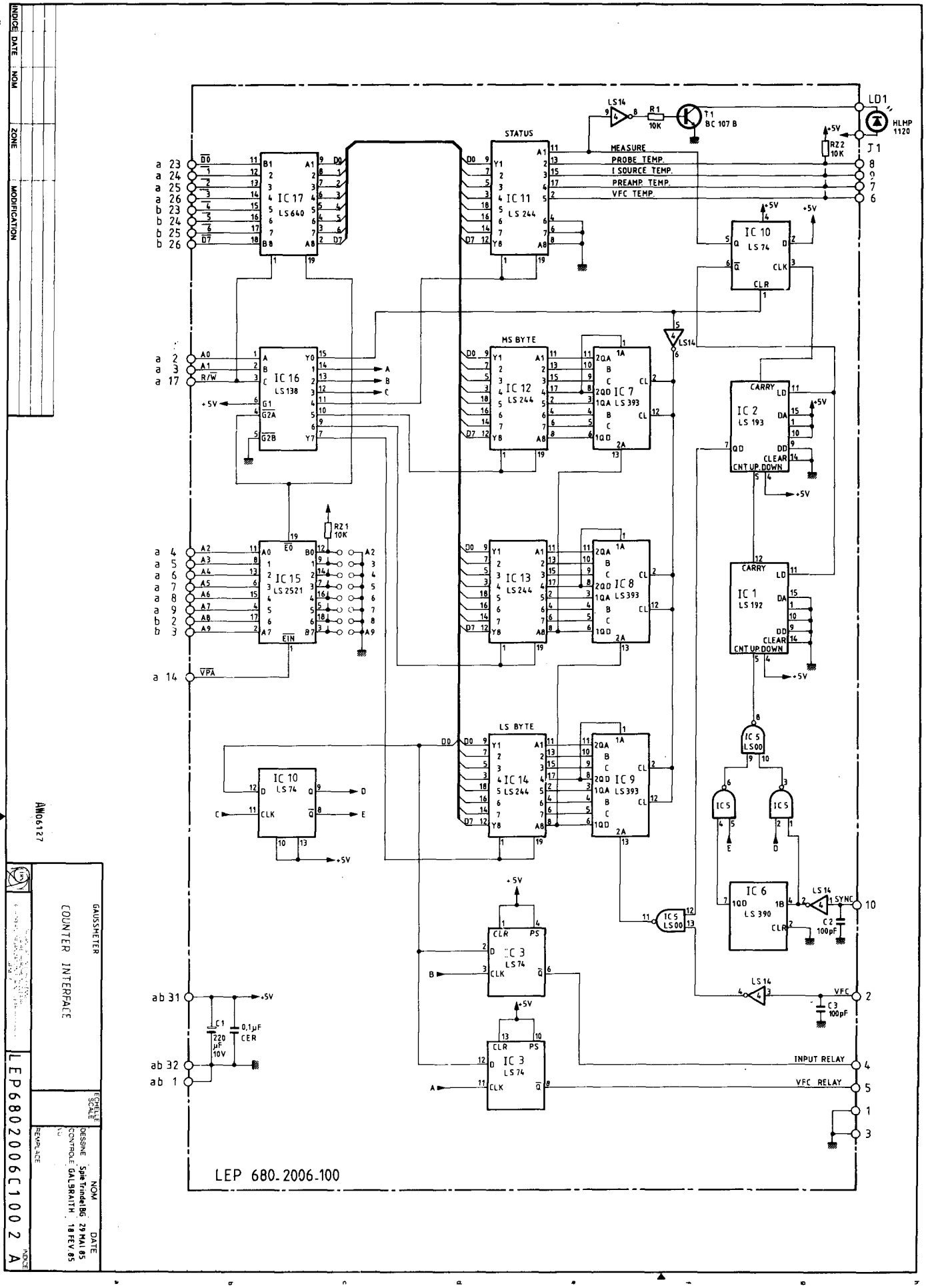
LEP6802006C2503 — INDICE A





GAUSSMETER	
COUNTER INTERFACE	
ECHELLE SCALE	
DESSINE	NOM Spé Trindel BG DATE 29 MAI 85
CONTROLE	GALBRAITH 18 FEV 85
REMPLACE	INDICE
LEP6802006C1002	A

INDICE | DATE | NOM | ZONE | MODIFICATION